IN THE CLAIMS

1. A method for fabricating an integrated circuit having at least one metallization plane, comprising

applying a first dielectric layer, a second dielectric layer, a third dielectric layer and a fourth dielectric layer to a surface of a substrate, in each case the first dielectric layer and the third dielectric layer, and the second dielectric layer and the fourth dielectric layer having the same etching properties and the thickness of the second dielectric layer differing from the thickness of the fourth dielectric layer,

using a first etching mask, which defines the arrangement of contact holes, if the thickness of the second dielectric layer is greater than the thickness of the fourth dielectric layer, etching is effected through the fourth dielectric layer and the third dielectric layer into the second dielectric layer thereby forming a hole, wherein a distance between the bottom of the hole and the upper face of the first layer is essentially equal to the thickness of the fourth dielectric layer, and, if the thickness of the fourth dielectric layer is greater than the thickness of the second dielectric layer, etching is effected into the fourth dielectric layer thereby forming a hole, wherein a distance between the bottom of the hole and the upper face of the first layer is essentially equal to the thickness of the second dielectric layer,

using a second etching mask, which defines the arrangement of line trenches, firstly a non-selective etching process is carried out, by means of which etching is effected into the fourth dielectric layer and the second dielectric layer without the surface of the underlying third dielectric layer and first dielectric layer being uncovered, and then the fourth dielectric layer and the second dielectric layer are etched selectively with respect to the third dielectric layer and selectively with respect to the first dielectric layer until the underlying surfaces of the first and of the third dielectric layer are uncovered in each case,

etching the third dielectric layer and the first dielectric layer until the underlying surface is uncovered in each case,

producing metal-containing contacts and lines of the metallization plane in the contact holes and in the line trenches.

2. The method of claim 1, further comprising the etching of the fourth dielectric layer, of the third dielectric layer and of the second dielectric layer using the first etching mask with the aid of a non-selective etching process.

3. The method of claim 1, further comprising the first dielectric layer and the third dielectric layer, and the second dielectric layer and the fourth dielectric layer, having essentially the same material composition.

4. The method of claim 2, further comprising comprising the first dielectric layer and the third dielectric layer, and the second dielectric layer and the fourth dielectric layer, having essentially the same material composition.

5. The method of claim 3, wherein the first dielectric layer and the third dielectric layer contain Si_3N_4 and the second dielectric layer and the fourth dielectric layer contain SiO_2.

6. The method of claim 1, in which the first dielectric layer and the third dielectric layer have essentially the same thickness.

7. The method of claim 1, in which the contacts and interconnects are formed by the deposition and planarization of metal.

8. The method of claim 1, in which the contacts and the interconnects contain copper.

9. The method of claim 1, in which the contacts contain copper.

10. The method of claim 1, in which the interconnects contain copper